Contact: 866-275-6964

support@ni.com



Terms and Definitions

The process of completely removing power from the device and its components and allowing for adequate discharge. This process includes a complete shutdown of the PC and/or chassis containing the device; a reboot is not sufficient for the completion of this process.

Requires power to maintain the stored information. When power is removed from this memory, its contents are lost. This type of memory typically contains application specific data such as capture waveforms.

Power is not required to maintain the stored information. Device retains its contents when power is removed. This type of memory typically contains information necessary to boot, configure, or calibrate the product or may include device power up states.

The component is read and/or write addressable such that a user can store arbitrary information to the component from the host using a publicly distributed NI tool, such as a Driver API, the System Configuration API, or MAX.

The component is read and/or write addressable from the host without the need to physically alter the product.

Per NIST Special Publication 800-88 Revision 1, "clearing" is a logical technique to sanitize data in all User Accessible storage locations for protection against simple non-invasive data recovery techniques using the same interface available to the user; typically applied through the standard read and write commands to the storage device.

Per NIST Special Publication 800-88 Revision 1, "sanitization" is a process to render access to "Target Data" on the media infeasible for a given level of effort. In this document, clearing is the degree of sanitization described.

NI 781xR, NI 783xR, NI PXI-784xR, NI PXI-785xR NEW!

- Onboard FPGA chip, programmable with the LabVIEW FPGA Module
- User-defined triggering, timing, and decision making in hardware with 25 ns resolution
- Up to 8 analog inputs, independent sampling rates up to 750 kHz, 16-bit resolution
- Up to 8 analog outputs, independent update rates up to 1 MHz, 16-bit resolution
- Up to 160 digital lines configurable as inputs, outputs, counters, or custom logic at rates up to 40 MHz
- Direct memory access (DMA) channels for high-speed data streaming
- Implement custom control logic inline signal processing, and digital communication protocols

Operating Systems

- Windows XP/2000
- LabVIEW Real-Time

Recommended Softv

- LabVIFW
- LabVIEW FPGA Module
- LabVIEW code compiler for FPGAs
- Emulated debugging mode
- . LahVIFW Real-Time Module

Driver Software (included)



Calibration Certificate Available

Product	Bus/Form Factor	FPGA	Analog Inputs (16-Bit)	Max Sampling Rate per Channel (kS/s)	Analog Outputs (16-Bit)	Max Update Rate per Channel (MS/s)	Digital I/O
Aultifunction R Serie	18						
NI 7851R	PXI	Virtex-5 LX30	8	750	8		96
NI 7852R	PXI	Virtex-5 LX50	8	750	8	1	96
NI 7853R	PXI	Virtex-5 LX85	8	750	8	1	96
NI 7854R	PXI	Virtex-5 LX110	8	750	8	1	96
NI 7841R	PXI	Virtex-5 LX30	8	200	8	1	96
NI 7842R	PXI	Virtex-5 LX50	8	200	8	1	96
NI 7830R	PCI, PXI	Virtex-II 1M gates	4	200	4	1	56
NI 7831R	PCI, PXI	Virtex-II 1M gates	8	200	8	1	96
NI 7833R	PCI, PXI	Virtex-II 3M gates	8	200	8	1	96
Digital R Series	FCI, FAI	VIII LEX-III SIVI Gates					
	DOL DVI	Virtex-II 1M gates		_	_		160
NI 7811R	PCI, PXI	Virtex-II 1M gates	BELLEVIN BUT THE		A DESCRIPTION OF THE PARTY OF		160

Table 1. R Series Selection Guide

Overview

Intelligent DAQ is multifunction data acquisition that features userdefined onboard processing as well as complete flexibility of I/O timing and triggering. You can configure all device functionality by creating NI LabVIEW block diagrams with the LabVIEW FPGA Module. Your block diagram executes in hardware, giving you direct, immediate control of all I/O signals on the PXI or PCI device. With R Series and LabVIEW FPGA, you can configure user-defined hardware for a wide variety of applications requiring precise timing and control such as:

- Data acquisition with flexible triggering and onboard processing
- · High-speed analog and discrete control loops
- · Pulse-width modulation (PWM) and encoder interfacing
- User-defined digital communication protocols
- · Custom counters with up to 64-bit resolution · Hardware-timed decision making at 40 MHz

Key Features

Through programming in LabVIEW FPGA, you can control each of the I/O signal lines independently or synchronize a line with other channels. You can configure the digital I/O lines as custom counter/timers, PWM channels, or communication buses for user-defined protocols. All multifunction R Series devices have dedicated analog-to-digital converters/digital-to-analog converters on every analog I/O channel. This offers specialized functionality such as multirate sampling and individual channel triggering, which are beyond the capabilities of typical data acquisition hardware. You can sample every analog input channel on an R Series device simultaneously at rates up to 750 kHz, and you can program every analog output on an R Series device to update simultaneously at rates up to 1 MHz. You can also store your compiled LabVIEW FPGA application in the onboard flash memory of any R Series device and configure it for automatic loading and/or execution at power up.



New Virtex-5 FPGAs

The new NI PXI-784xR and PXI-785xR modules use new Virtex-5 field-programmable gate arrays (FPGAs) with improved optimization capabilities that provide faster code execution and increased code capacity. These Virtex-5 FPGAs feature a new six-input lookup table (LUT) architecture for substantially improved resource utilization as well as DSP48 slices that make it possible for you to implement more complex digital signal processing at faster rates. Previous-generation Virtex-II FPGAs use four-input LUTs for up to 16 combinations of digital logic values. The new Virtex-5 FPGAs use six-input LUTs for up to 64 combinations, increasing the amount of logic that you can implement per slice. In addition, the slices themselves are placed in closer proximity to each other to reduce the propagation delay of electrons and increase overall execution rates. The single-cycle timed loop structure in LabylEW FPGA takes full advantage of six-input LUTs for substantially improved resource utilization. This means you can optimize more LabylEW FPGA code to fit within Virtex-5 FPGAs and perform more operations per clock cycle.

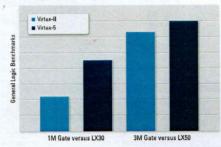


Figure 1. General logic benchmarks show that Virtex-5 FPGAs offer larger sizes when compared to Virtex-II FPGAs.

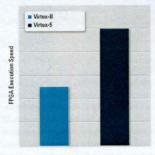


Figure 2. Execution speed benchmarks show that Virtex-5 FPGAs feature faster processing capabilities when compared to Virtex-II FPGAs.

For more information on LabVIEW FPGA benchmarks for Virtex-5 FPGAs, visit ni.com/info and enter lvfpgabenchmarks.

Recommended Accessories

High Performance

SHC68-68-RMIO — High-performance shielded 68-conductor cable terminated with a VHDCI 68-pin male connector at one end and a 68-pin female 0.050 D-type connector at the other end that has been specifically designed for the multifunction I/O connector on R Series intelligent DAQ devices.

1	m	189588-01
2	m	189588-02

SHC68-68-RDIO — High-performance shielded 68-conductor cable terminated with a VHDCI 68-pin male connector at one end and a 68-pin female 0.050 D-type connector at the other end that has been specifically designed for the digital I/O connector on R Series intelligent DAQ devices.

1 m191667-01

SCB-68 — Shielded I/O connector block for rugged, very low-noise signal termination for connecting to 68-pin devices. The SCB-68 also includes two general-purpose breadboard areas.

Dimensions - 19.5 by 15.2 by 4.5 cm (7.7 by 6.0 by 1.8 in.)

SCB-68776844-01

Low Cost

SH68-C68-S — General-purpose shielded cable that connects any type of R Series connector to 68-pin connector blocks.

0.5 r	n186381-0R5
1 m	186381-01
2 m	186381-02

Custom Cabling

SHC68-NT-S — Shielded 68-conductor cable terminated with a 68-pin male VHDCI connector at one end and unterminated bare wires at the other. Use this cable, ideal for OEM applications, to create custom cabling solutions for R Series devices.

2 m189041-02

NSC68-262650 — Shielded cable terminated with a VHDCI 68-pin male connector at one end and two 26-pin ribbon connectors and one 50-pin ribbon connector on the other; designed to connect the R Series RMIO connector to standard ribbon cable accessories.

1 m189151-01

NSC68-5050 — Shielded cable terminated with a VHDCI 68-pin male connector at one end and two 50-pin ribbon connectors on the other; designed to connect R Series RDIO connectors to standard ribbon cable accessories.

1 m189152-01

Required Software for R Series Intelligent DAQ

- NI 781xR and 783xR devices require the LabVIEW FPGA Module 7.1 or later and NI-RIO 1.3 or later driver software.
- NI 784xR and 785xR devices require the LabVIEW FPGA Module 8.5.1 or later and NI-RIO 2.4 or later.
- NI 7853R and 7854R devices require the LabVIEW FPGA Module 8.6 or later and NI-RIO 3.0 or later.

Low-Cost Signal Conditioning and Channel Expansion

The NI cRIO-9151 R Series expansion chassis connects directly to any digital connector on R Series devices and houses up to four C Series I/O modules for industrial signal conditioning, I/O channel expansion, and direct sensor connectivity.

Ordering Information

PCI	
	770000 04
NI PCI-7811R	
NI PCI-7813R	779370-01
NI PCI-7830R	779361-01
NI PCI-7831R	778797-01
NI PCI-7833R	779359-01
PXI	
NI PXI-7811R	778800-01
NI PXI-7813R	779362-01
NI PXI-7830R	779364-01
NI PXI-7831R	778668-01
NI PXI-7833R	779360-01
NI PXI-7841R	780337-01
NI PXI-7842R	780338-01
NI PXI-7851R	780339-01
NI PXI-7852R	780340-01
NI PXI-7853R	780341-01
NI PXI-7854R	780342-01
Includes NI-RIO driver software.	

BUY NOW!

For complete product specifications, pricing, and accessory information, call 800 813 3693 (U.S.) or go to ni.com/rseries.

Specifications

Analog Input (NI 783xR/784xR/785xR Only)

Input Characteristics

Number of channels	
NI 7830R	4
NI 7831R/7833R/784xR/785xR	8
Input modes	DIFF, RSE, NRSE
	(software-selectable; selection applies to all channels)
Type of ADC	Successive approximation
Resolution	16 bits, 1 in 65,536
Conversion time	
NI 783xR/NI 784xR	4 µs
NI 785xR	1 µs
Maximum sampling rate	
NI 783xR/NI 784xR	200 kS/s (per channel)
NI 785xR	750 kS/s (per channel)
Input impedance	
Powered on	10 GΩ in parallel with 100 pF
Powered off/overload	4.0 kΩ min
Input signal range	±10 V
Input bias current	
NI 783xR	±2 nA
NI 784xR/785xR	±5 nA
Input offset current	
NI 783xR	±1 nA
NI 784xR/785xR	±5 nA
Input coupling	DC
Maximum working voltage	
(signal + common mode)	Inputs should remain
	within ±12 V of ground
Overvoltage protection	
Powered on	
Powered off	±35 V
Data transfers	DMA, interrupts, programmed

Accuracy Information - NI 783xR

DE ANDRES	WHITE ST	10000	200	Abs	olute	Accuracy			Relative	Accuracy
Nominal Range (V)		% of R	eading		Noise + Quantization				Resolution (µV)	
Positive Full Scale	C. 11	24	1 Year	Offset (M)	Single Point	Averaged	Temp Drift (%/°C)	at Full Scale (±mV)	Single Point	Averaged
10.0	-10.0	0.0496	0.0507	2,542	1779	165 ing an intern	0.0005		2,170	217

10.0 -10.0 0.0499 0.0507 (2.742 1773 in 3.00005 7.70 2.777 2.777 Note: Accuracies are valid for measurements following an internal calibration. Averaged numbers assume ditheting and averaging of 100 single-channel roadings. Measurement accuracies are listed for operational temperatures within ±1 °C of internal calibration temperature and ±10 °C of external or

Accuracy Information — NI 784xR/785xR

Audui	401 .			-	1000					
-	WEST THE	SECTION.	(6.20)	Abs	solute /	Accuracy			Relative	Accuracy
Nominal Range (\		% of R	eading	Noise +				Resolution (µV)		
Positive Full Scale			1 Year	Offset (M)	Single Point	Averaged	Temp Drift (%/°C)	Scale	Single Point	Averaged
10.0		0.0186					0.0005		1,205	121

Note: Accuracies are valid for measurements following an internal calibration. Averaged numbers assume dithering and averaging of 100 single-channol readings. Measurement accuracies are allisted if operational temperatures within ±1 °C of internal calibration temperature and ±10 °C of external or

DC Transfer Characteristic

De Italisier characteristics	
INL	
NI 783xR	±3 LSB typ, ±6 LSB max
NI 784xR/785xR	±1 LSB typ, ±3 LSB max
DNL	
NI 783xR	-1.0 to +2.0 LSB max
NI 784xR/785xR	±0.4 LSB typ, ±0.9 LSB max
No missing codes	
NI 783xR	16 bits typ, 15 bits min
NI 784xR/785xR	16 bits guaranteed
CMRR, DC to 60 Hz	-86 dB

Settling Time

SCHOOL STORY		Accuracy				
Device	Step Size	16 LSB	4 LSB	2 LSB		
	±20.0 V	7.5 µs	10.3 µs	40 µs		
NI 783xR	±2.0 V	2.7 µs	4.1 µs	5.1 µs		
	±0.2 V	1.7 µs	2.9 µs	3.6 µs		
	±20.0 V	2.1 µs	4.2 µs	8 µs		
NI 784xR/	±2.0 V	1.3 µs	1.6 µs	1.8 µs		
785xR	±0.2 V	0.8 μs	1.1 us	1.2 µs		

Crosstalk.....-80 dB, DC to 100 kHz

Dynamic Characteristics

Dynamic Characteristics	
Bandwidth	
NI 783xR	
Small signal (-3 dB)	650 kHz
Large signal (1% THD)	55 kHz
NI 784xR/785xR	
Small signal (-3 dB)	1 MHz
Large signal (1% THD)	500 kHz

Analog Output (NI 783xR/784xR/785xR Only)

Output Characteristics

Number of channels	
NI 7830R	4
NI 7831R/7833R/784xR/785xR	8
Output type	Single-ended, voltage output
Resolution	16 bits, 1 in 65,536
Update time	1.0 µs
Maximum update rate	1 MS/s
Type of DAC	Enhanced R-2R
Data transfers	DMA, interrupts,
Duta daniero in initialization	programmed I/O

	TO DEED							
Voltage	Output	1					Protection	
Range		11		±10 V			Input	05 1 70 1/ - -
Output cou				DC			NI 781xR/783xR	
Output imi							NI 784xR/785xR	
	R			1.25 Ω			Output	
	R/785xR							may be shorted at a time
				±2.5 mA			Minimum pulse width	
Current dr				- 1000	cuit to gr	nund	Input	. 25 ns
							Output	. 12.5 ns
Power-on	state			User cor	nfigurable		Minimum sampling period	
Accura	cy Info	rmation					Reconfigurable FPGA	
			Absolute A	ccuracy				
Nominal Re	ange (V)	% of Re	ading		- 0.4	Absolute	NI 7811R/7830R/7831R	
Positive	Negative			Offset (µv)	(%/°C)	Accuracy at Full Scale (mV)	FPGA type	Virtex-II 1000
Full Scale	Full Scale	24 Hours	1 Year				Number of flip-flops	10,240
10.0	-10.0	0.0335	0.0351	2,366	0.0005	5.88	Number of 4-input LUTs	
listed for oper	ration temperat	ures within ±	°C of interna	calibration ten	perature and ±	utput accuracies are 10 °C of external or	Number of 18x18 multipliers	
factory calibra	ation temperatu	ure. Temperatur	e drift applie	s only if ambient	is greater than	n ±10 °C of previous	Embedded block RAM	
external calibration.						NI 7813R/7833R	/20 10	
DC Trai	nsfer Cl	haracte	ristics					Vistory II 2000
INL				+0.5 LSI	3 tvp. ±4.0	LSB max	FPGA type	
DNL					3 typ. ±1 l		Number of flip-flops	
					guarante		Number of 4-input LUTs	
MONOTORIO	city			TO DIES,	guarante		Number of 18x18 multipliers	96
Settling	g Time						Embedded block RAM	1,728 kb
				Accura		2 LSB	NI 7841R/7851R	
Step :		16 LS 6.0 μ	TERROR STREET,	4 LSB 6.2 μs		7.2 us	FPGA type	Virtex-5 LX30
±20.0		2.2 µ		2.9 µs		3.8 µs	Number of flip-flops	
±0.2		1.5 µ		2.6 µs		3.6 µs	Number of 6-input LUTs	
							Number of DSP48	
Dynam	ic Char	acteris	tics				slices (25x18 multipliers)	32
Slew rate				10 V/µs			Embedded block RAM	
					ms, DC to	1 MHz	Embedded block nAM	1,132 KD
	ergy at mid				V for 3 µs		NI 7842R/7852R	
GIIICH ene	ary at miu	iscale trail	310011	1200 111	v 101 5 μ5			Virtex-5 LX50
Digital	1/0						FPGA type	
	of channel	S					Number of flip-flops	
	1R/7813R			160			Number of 6-input LUTs	28,800
100000000000000000000000000000000000000							Number of DSP48	
	0R						slices (25x18 multipliers)	
	1R/7833R				TI CVII	Compatible	Embedded block RAM	1,728 kb
Digital lo	gic levels			3.3 V T	IL, 5 V 11	L Compatible	NI 70E3D	
District Street	Leve			Min (V)		Max (V)	NI 7853R	VC - FLVOF
Marie Control of the	Input low vol	tage (V _{IL})		0.0 V		0.8 V	FPGA type	
1	Input high vol	tage (V _{IH})		2.0 V		5.5 V	Number of flip-flops	
0	utput low vol			10.		0.4 V	Number of 6-input LUTs	51,840
-	where lour =					224	Number of DSP48	
OL	where lour			2.4 V		3.3 V	slices (25x18 multipliers)	48
	Where lour	= 4 1104					Embedded block RAM	
Output cu	urrent							
	·			. 4.0 mA			NI 7854R	
000.00							FPGA type	Virtex-5 LX110
	kage curre						Number of flip-flops	69,120
				or the same of	nmable, b	ny lina	Number of 6-input LUTs	
	state						Number of DSP48	
Data tran	nsfers				nterrupts,		slices (25x18 multipliers)	64
				program	nmed I/O		Embedded block RAM	

Timebases		Maximum Working Voltage			
Timebase reference sources		Maximum working voltage refers to th	e signal voltage plus the		
NI PCI-781xR/783xR	Onboard clock only	common-mode voltage.			
NI PXI-78xxR	Onboard clock, phase-locked to	Channel-to-earth			
	PXI 10 MHz clock	Channel-to-channel	±24 V, Measurement Category I		
LabVIEW FPGA derived clocks	Up to 200 MHz	Caution: Do not use the NI 783xR/784	vR/785vR for connection to		
Timebase accuracy, onboard clock	±100 ppm, 250 ps	signals in Measurement Category II, III, or IV.			
	peak-to-peak jitter	signals in Weasurement Category II, III	, 01 14.		
Phase-locked to PXI 10 MHz clock		Power Requirement			
(NI PXI-78xxR only)	Adds 350 ps peak-to-peak jitter	+5 VDC (±5%)1			
Additional frequency-dependent peak-	to-peak jitter	NI 781xR	9 mA (typ), 50 mA (max)		
NI 781xR/783xR		NI 7830R/7831R	330 mA (typ), 355 mA (max)		
40 MHz	None	NI 7833R	364 mA (typ), 586 mA (max)		
80 MHz		NI 7841R/7851R	125 mA (typ), 252 mA (max)		
120 MHz	720 ps	NI 7842R/7852R	136 mA (typ), 291 mA (max)		
160 MHz		NI 7853R.	460 mA typ		
200 MHz	700 ps	NI 7854R	484 mA typ		
NI 784xR/785xR		+3.3 VDC (±5%)2			
40 MHz	None	NI 7811R	650 mA (typ), 1,000 mA (max)		
80 MHz		NI 7813R	850 mA (typ), 1,350 mA (max)		
120 MHz	172 ps	NI 7830R/7831R	462 mA (typ), 660 mA (max)		
Calibration (NI 783xR/784xR/785xR Only)		NI 7833R	727 mA (typ), 1,148 mA (max)		
Recommended warm-up time	15 minutes	NI 7841R/7851R	525 mA (typ), 1,244 mA (max)		
Calibration interval	1 year	NI 7842R/7852R	604 mA (typ), 1,484 mA (max)		
Onboard calibration reference		NI 7853R	640 mA typ		
DC level	5,000 V (±3.5 mV) (actual value	NI 7854R	843 mA typ		
	stored in flash memory)	+12 V			
Temperature coefficient	±5 ppm/°C max	NI 784xR/785xR	0.5 A		
Long-term stability		-12 V			
N - D O		NI 784xR/785xR	0.25 A		
Note: Refer to Calibration Certificates		+5 V terminal			
generate a calibration certificate for the	ie NI /83XH.	Connector 0			
Bus Interface		Connector 1			
PXI (NI PXI-78xxR only)	Master, slave	Connector 2			
PCI (NI PCI-781xR/783xR only)	Master, slave	All connectors			
	iviastei, siave	To calculate the total current sourced by the digital outputs, use			
Physical		the following equation:			
Dimensions (not including connectors)		√j			
NI PCI-781xR/783xR	17 by 11 cm (6.7 by 4.3 in.)	∑ current sourced on channel			
NI PXI-78xxR	16 by 10 cm (6.3 by 3.9 in.)		A FO to F OF VDC at 1 A total		
Weight		Power available at I/O connectors			
NI PCI-781xR/783xR	112 g		250 mA per I/O connector pin		
NI PXI-78xxR	152 g	Does not include current drawn from the +5 V line on the I/O connectors.			
I/O connectors		² Does not include current sourced by the digital outputs.			
NI 781xR	Four 68-pin female	³ The NI 784xR/785xR devices have a user-replaceable socketed fuse that opens when cuexceeds the current specification. Refer to the R Series Intelligent DAQ User Manual, at			
	high-density VHDCI type	at ni.com/manuals, for information about fuse replacement.			
NI 783xR/784xR/785xR	Three 68-pin female				
	high-density VHDCI type				

Environmental

NI 78xxR devices are intended for indoor use only.

Operating Environment

NI 701AII.	accordance with IEC-60068-2-1 and IEC-60068-2-2)
NI 7830R, NI 7831R	
40 or 80 MHz timebase	0 to 55 °C (tested in accordance with IEC-60068-2-1 and IEC-60068-2-2)
NI 7833R/7841R/7842R/7851R/7852R/	/7853R/7854R
, 40 MHz timebase	0 to 55 °C (tested in accordance with IEC-60068-2-1 and IEC-60068-2-2)
80 MHz timebase	0 to 55 °C except the following: 0 to 45 °C when installed in an NI PXI-1000/B or NI PXI-101x (tested in accordance with IEC-60068-2-1 and IEC-60068-2-2)
Relative humidity range	10 to 90%, noncondensing (tested in accordance with IEC-60068-2-56)
Altitude	2,000 m at 25 °C

Note: Clean the device with a soft, nonmetallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

Shock and Vibration (for NI PXI-78xxR Only)

Safety and Compliance

Safety

NI 78xxR devices are designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note: For UL and other safety certifications, refer to the product label or visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326 (IEC 61326): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Note: Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

National Instruments is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial not only to the environment but also to NI customers.

For additional environmental information, refer to the NI and the Environment Web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers: At the end of their life cycle, all products must be sent to a WEEE recycling center. For more information about WEEE recycling centers and National Instruments WEEE initiatives, visit ni.com/environment/weee.htm.

电子信息产品污染控制管理办法(中国 RoHS)

 ● 中国客户 National Instruments 符合中国电子信息产品中限制使用某些有等地長期 中 (RoHS)。 关于 National Instruments 中国 RoHS 会積性信息。 連盟条 nal.com/serviz reseasor/ robus_chizea. (For information about China RoHS compliance, go to nal.com/servizoreasor/robus_chizea).

NI Services and Support



NI has the services and support to meet your needs around the globe and through the application life cycle — from planning and development through deployment and ongoing maintenance. We offer services and service levels to meet customer requirements in research, design, validation, and manufacturing. Visit ni.com/services.

Training and Certification

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Professional Services

Our NI Professional Services team is composed of NI applications and systems engineers and a worldwide National Instruments Alliance Partner program of more than 600 independent consultants and



integrators. Services range from start-up assistance to turnkey system integration. Visit ni.com/alliance.

OEM Support

We offer design-in consulting and product integration assistance if you want to use our products for OEM applications. For information about special pricing and services for OEM customers, visit ni.com/oem.

Local Sales and Technical Support

In offices worldwide, our staff is local to the country, giving you access to engineers who speak your language. NI delivers industry-leading technical support through online knowledge bases, our applications engineers, and access to 14,000 measurement and automation professionals within NI Developer Exchange forums. Find immediate answers to your questions at ni.com/support.

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Hardware Services

NI Factory Installation Services

NI Factory Installation Services (FIS) is the fastest and easiest way to use your PXI or PXI/SCXI combination systems right out of the box. Trained NI technicians install the software and hardware and configure the system to your specifications. NI extends the standard warranty by one year on hardware components (controllers, chassis, modules) purchased with FIS. To use FIS, simply configure your system online with ni.com/pxiadvisor.

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NI recognizes the need to maintain properly calibrated devices for high-accuracy measurements. We provide manual calibration procedures, services to recalibrate your products, and automated calibration software specifically designed for use by metrology laboratories. Visit ni.com/calibration.

Repair and Extended Warranty

NI provides complete repair services for our products. Express repair and advance replacement services are also available. We offer extended warranties to help you meet project life-cycle requirements. Visit ni com/services.



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Manufacturer: National Instruments

Roard Assembly Part Numbers (Refer to Procedure 1 for identification procedure):

Dual a Assembly 1 art 1 am	Bers (Refer to Treetment
Part Number and Revision	Description
192463A-01L or later	PCI-7811R
192463A-03L or later	PCI-7813R

Volatile Memory

Target Data	Type	Size	Battery Backup	User ¹ Accessible	System Accessible	Sanitization Procedure
Data storage during	FPGA	40 x 18 Kbits (-01)	No	Yes	Yes	Cycle Power
VI execution	Block	96 x 18 Kbits (-03)				
77 0700 0111011	RAM					

Non-Volatile Memory (incl. Media Storage)

Target Data	Туре	Size	Battery Backup	User Accessible	System Accessible	Sanitization Procedure
Device configuration Device information FPGA bitstream	FLASH	1M x 8 bits (-01) 2M x 8 bits (-03)	No	No Yes	Yes Yes	None Procedure 2
CPLD Configuration	CPLD	17KB	No	No	No	None

Refer to Terms and Definitions section for clarification of User and System Accessible





Procedures

Procedure 1 -Board Assembly Part Number Identification:
To determine the Board Assembly Part Number and Revision, refer to the label applied to the surface of your product. The Assembly Part Number should be formatted as "P/N: #####a-##L

Procedure 2 - Device Configuration Flash (FPGA bitstream):
You can use the NI-RIO Device Setup utility to erase the FPGA bitstream data. For more details, visit ni.com/info and enter the infocode fpgaflashclr.